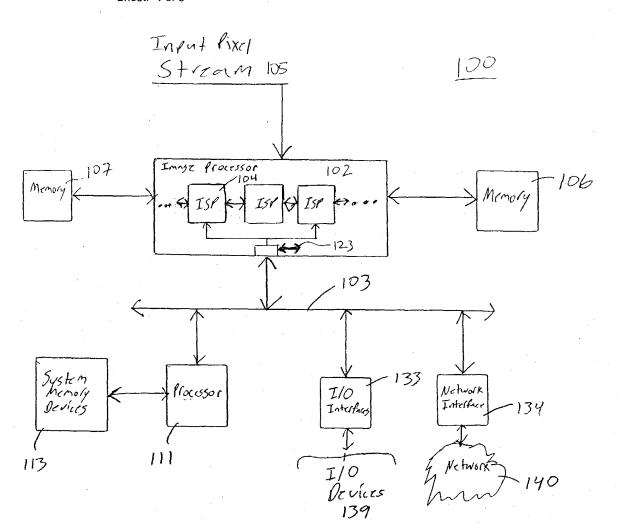
Blakely, Sokoloff, Taylor & Zafman LLP (714) 5
Title: Memory Command Handler for Use In An Image Signal
Processor Having A Data Driven Architecture
1st Named Inventor: Louis A. Lippincott (714) 557-3800

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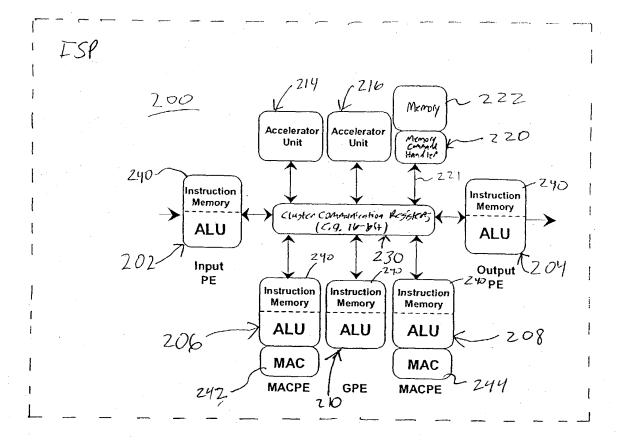


Figure Z

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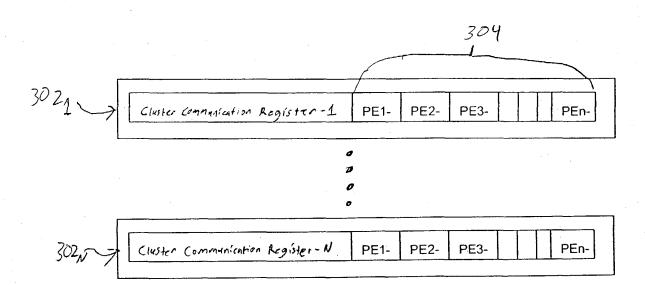


Figure 3

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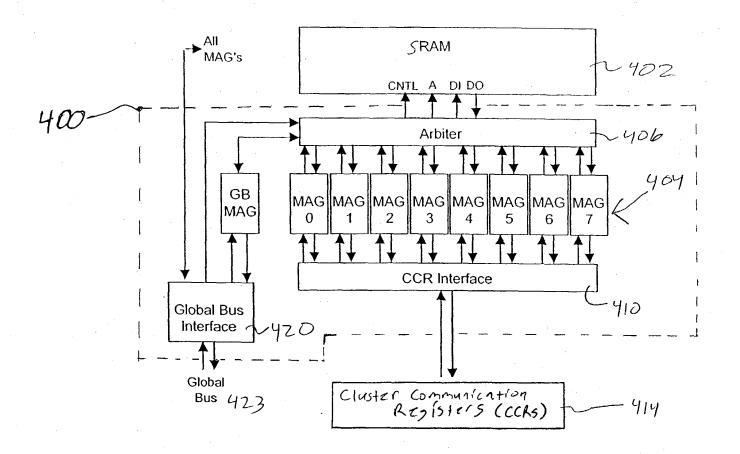
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MAG	MAG0	MAG1	MAG2	MAG3	MAG4	MAG5	MAG6	MAG7
CCKO CCR1 CCR2 CCR3 CCR4 CCR4 CCR5	Command							<u></u>
CCF!	Data						,	- · · · · · · · · · · · · · · · · · · ·
CCR2		Command						
CCF3		Data						
CCRU,			Command					
- CCR5			Data					
CCRE				Command				
CCR7				Data				
CCRT					Command			
CCKG					Data			
CCKIC	_ <del>-</del>					Command		
CCK;						Data		
CORT	-						Command	
CCKIZ							Data	
CCKIL		ļ						Comma
TCKIS	5]		<b>,</b>	]	1			Data

Figure 5

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Mask Register	2602
Data Path DV Bits Register	604
Base Offset Register	1606
Memory Pointer Register	658
Increment Register	-610
Increment Register	-612
Operation Complete Register	1-614
CONTROL Bits	
Control Bits	5614
0 6 0	
o o	
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MCH Command	Description			
Write Mask	Used in address calculations to create circular buffer addressing			
Set Data Path DV bits	Determines the target PE(s) for the read data			
Read Immediate	Reads RAM from a specified address			
Write Immediate	Writes RAM from the Data LLK to a specified RAM address			
Write MPR	An initial offset value to be used in address calculations			
Write Increment Register	Provides X and Y increment values for one or 2D addressing			
Write Base Offset Register	Sets the Base Offset Register used in addressing			
Read Indirect, N Words	Reads N words into the Data CCR using the MAG Memory Pointer			
Write Indirect, N Words	Writes N words from the Data CCK using the MAG Memory Pointed			
Read Op Complete	Used to signal the MCH control PE that a block transfer is complete			
Infinite Indirect Operation	Set infinite indirect MCH operation			

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15	14	13	12	11	10	9	8-0	
0	0	х	х	х	×	х	х	Read Immediate
1,	0 :	Х	Х	х	Х	х	X	Write Immediate
0	1	0	Х	Х	х	х	×	Read Indirect
0	1.	1	х	Χ.	х	×	х	Write Indirect
13	. 1ts.	· 0 ·	(1)	Х	Х	Х	х	Write Increment Registers
1.,	1.	0	0	0-	X	х	х	Set Data Path
1	1	0	0	1	0	0	х	Set Read Operation Complete
.13	.1	1.7	0.3	0.	х	Х	х	Write Memory Pointer Register
11/2	×.1.	1.	0	1.	х	х	х	Write Base Offset
		1		:02	х	х	х	Write Mask Register
1	1	1		1 2	Х	х	Х	Write First Use Registers

Figure 8